ISSN: 0974-2115
www.jchps.com Journal of Chemical and Pharmaceutical Sciences

A Comparative Study on CBL, COT, BEC Techniques Based Carry Select Adder

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ABSTRACT

Carry Select Adders (CSLAs) are broadly used in various operations since their carry propagation delay is low while analyzing with that of the other ordinary adders. The specialty of these CSLAs is that it uses a separate Carry selection unit which is usually a MUX that selects the appropriate output for the operation. Since these Carry Select Adders use two ripple carry adders for their operation, the area used by these adders becomes quite large. Hence several techniques have been proposed to improve the parameters of CSLAs and thereby reducing their CPD and power. Techniques like a using BEC unit instead of one of the RCAs in CSLA, using a Common logic unit instead of the repeated CSLA, COT based CSLA are proposed. All these techniques basically try to eliminate the repeated logic operations of the typical CSLA. In this paper, illustration of the various above mentioned techniques is given; also it provides a clear idea of which technique could be used to implement the efficient CSLA.

KEY WORDS: CSLA, CPD, BEC, COT.

1. INTRODUCTION

An adder is definitely an important processing unit as it forms the major component of several arithmetic units. More complex Digital Processing Units will use a large amount of adders to perform their function. Thus it becomes clear that an efficient adder design will definitely improve the performance of the Digital Processing units that uses these adders. The basic form of adder design used in many types of DSP subsystems is the frequently used Ripple carry adders design (RCA). These ripple carry adders are not much welcomed since the time taken by the carry to propagate is very high. The full adders that are used in the RCA design need to postpone its work until and unless the carry bit from the another full adder placed previous to it reaches it, to continue its function; which leads to the carry propagation delay (CPD) of this RCAs to become very high. Hence there comes a need for the search of other efficient adders than RCAs that can provide a better performance. The answer will be Carry Select Adders (CSLA).

The basic CSLA design includes the combination of two RCAs that are used in the CSLA architecture. Both of the RCAs present in the design calculate the sum bits for the inputs provided. Even though the CSLAs provide less propagation delay for the carry bit than the RCAs, there is a drawback in CSLA design that has to be also considered. The major drawback in the CSLA design is the presence of duality in the RCA network. Since these Carry Select adders use two ripple carry adders for their operation, the area used by these adders becomes quite large. To avoid this, various techniques were suggested that include replacing one of the RCAs. The techniques suggested optimizing the CSLA design is discussed one by one. In fig.1the CSLA design is shown.

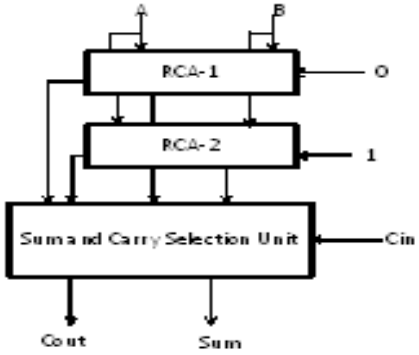

Figure.1.CSLA

2. METHODS AND MATERIALS OF CSLA

BEC Based CSLA: Since the major drawback in the CSLA design is the presence of duality in the RCA network, this can be greatly neglected by using the BEC including design for CSLA. In the BEC based CSLA design, a qualified method for the CSLA can be obtained by using a BEC unit instead of one of the RCAs. By using this design technique, the propagation time for the carry bit in the CSLA is reduced considerably. Hence this technique is preferred and used for the CSLA implementation. In the fig.2.BEC related CSLA design is shown. One of the demerits of this technique is that the area increases; size of the adder increases. So, we go for another technique called CBL based CSLA.

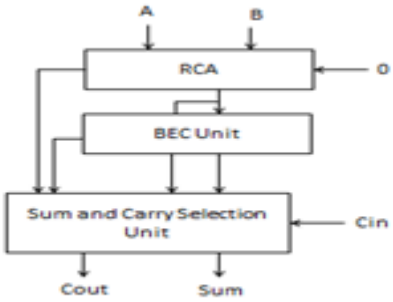

Figure.2. BEC based CSLA

CBL Based CSLA: In CBL based CSLA design, the CSLA shares the Boolean logic that is common to both the RCAs; the logic expression used to find the sum is same for both the RCAs used in the CSLA. So, if that Boolean logic function can be shared then there will be no need for obtaining dual sum outputs using both RCAs. Since the common Boolean logic is shared, a tantamount sum and carry outputs can be produced. This method of producing the tantamount sum and carry bits can greatly reduce the area, delay and power as well for the CSLA implementation.

COT Based CSLA: COT stands for Carry Optimization Technique. In the COT based design for CSLA, the entire architecture of the CSLA is broken down into carry selection and generation unit. The HSG unit performs the half sum of the inputs provided. The FSG unit calculates the final full Sum. In the fig.3.the block diagram for carry optimization technique is shown.

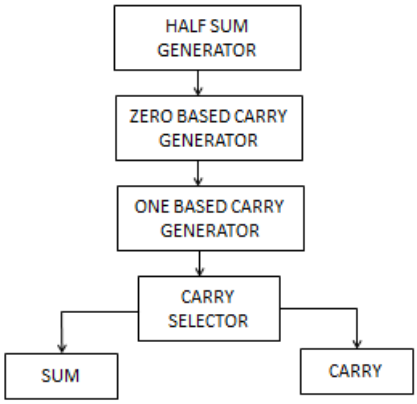

Figure.3. Block diagram for COT based CSLA.

3. RESULTS AND DISCUSSION

From the various techniques discussed so far, it is clear to demonstrate that the COT technique will be the appropriate technique used to implement the effective CSLA. The coding for the COT technique is written and run in Xilinx software. The simulation result is shown in the figure.

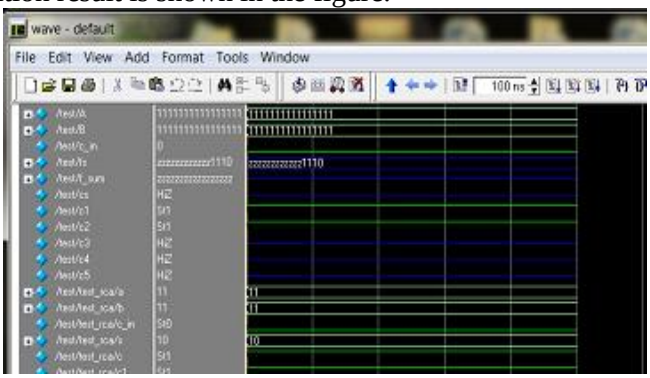

Figure.4. Simulation result for carry optimized CSLA

In fig.4. The simulation result for the proposed carry optimized CSLA is shown using the Modelsim software. In fig.5.the power analysis of the COT based CSLA is calculated using Xilinx software. In fig.6.the delay analysis for the COT based CSLA is shown.

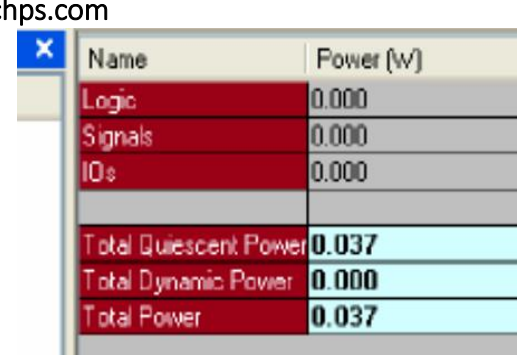

Figure.5. Power analysis of COT based CSLA

Cell:in->out	fanout	Gate Delay
IBUF:I->O	2	0.821
LUT3:I0->O	2	0.551
LUT3:I1->O	1	0.551
OBUF:I->O		5.644
Total		10.656ns

Figure.6. Delay analysis of the COT based CSLA

4. CONCLUSION

From the various available techniques like CBL,BEC,COT that are discussed, it is clear to demonstrate that the COT technique will be the appropriate technique used to implement the effective CSLA. Implementation of CSLA with the COT technique greatly reduces the power, improves the speed and less area is used. The future work deals with further consideration to reduce the number of logic gates used for the carry select adder and thus to reduce the power consumption of the circuit; also the FPGA implementation of the highly efficient carry select adder.

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